PIN-array - halfbridge driver SKiiP 2, 3 GB 2, 3, 4-fold

X1:

Pin	signal	remark
1	shield	
2	BOT IN[2)]	positive 15V CMOS logic; 10 kΩ impedance, don´t connect when using fiber optic
3	ERROR OUT[1)]	LOW = NO ERROR; open Collector Output; max. 30 V / 15 mA don´t connect when using fiber optic, propagation delay 1 µs min. pulsewidth error-memory-reset 9 µs
4	TOP IN[2)]	positive 15V CMOS logic; 10 kΩ impedance don´t connect when using fiber optic
5	Overtemp. OUT[1)]	LOW = NO ERROR = ϑ_{DCB} < 115 ± 5°C open collector Output; max. 30 V / 15 mA „low“ output voltage < 0,6 V „high“ output voltage max. 30 V
6	+ 24 V_{DC} IN	24 V_{DC} (SKiiP 2: 20 - 30 V, SKiiP 3: 13 - 30 V)
7	+ 24 V_{DC} IN	don´t supply with 24 V, when using + 15 V_{DCIN} supply voltage monitoring threshold 19,5 V
8	+ 15 V_{DC} IN (SKiiP 2 only)	15 V_{DC} ± 4 % power supply
9	+ 15 V_{DC} IN (SKiiP 2 only)	don´t supply with 15 V, when using + 24 V_{DCIN} supply voltage monitoring threshold 13 V
8	+ 15 V_{DC} OUT	max. 50 mA auxiliary power supply when
9	+ 15 V_{DC} OUT	SKiiP system is supplied via pin 6/7
10	GND	GND for power supply and
11	GND	GND for digital signals
12	Temp. analog OUT or U_{DC} analog OUT[3)]	U_{DC} when using option “U” actual DC-link voltage, 9 V refer to U_{DCmax} max. output current 5 mA; overvoltage trip level 9 V
13	GND aux	reference for analog output signals
14	I analog OUT	**SKiiP 2 and SKiiP 3 with Al_2O_3 ceramic substrate** current actual value 8,0 V ⇔ 100 % I_C @ 25 °C overcurrent trip level 10 V ⇔ 125 % I_C @ 25 °C current value > 0 ⇔ SKiiP system is source current value < 0 ⇔ SKiiP system is sink **SKiiP 3 with AlN ceramic substrate:** refer to corresponding datasheet

[1)] Open collector output, external pull up resistor necessary
[2)] „high“ (min) 11,2 V, „low“ (max) 5,4 V; SKiiP 3: 1 nF capacitance added signal to GND
[3)] When using option “U” the analog temperature signal is not available

PIN-array - single phase bridge driver SKiiP2 type „GH”

X1:

Pin	signal	remark
1	shield	
2	BOT HB 1 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
3	TOP HB 1 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
4	BOT HB 2 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
5	TOP HB 2 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
6	Ground fault protection	0V: Disable not connected: ENABLE
7	Overtemp. OUT [1)]	LOW = NO ERROR = ϑ_{DCB} < 115 ± 5°C open collector Output; max. 30 V / 15 mA „low“ output voltage < 0,6 V „high“ output voltage max. 30 V
8	ERROR OUT [1)]	LOW = NO ERROR; open collector Output; max. 30 V / 15 mA propagation delay 1 µs, min. pulsewidth error-memory-reset 8 µs
9	GND	GND for power supply and
10	GND	GND for digital signals
11	+ 15 V_{DC} IN	15 V_{DC} ± 4 % power supply
12	+ 15 V_{DC} IN	don´t supply with 15 V, when using + 24 V_{DCIN} supply voltage monitoring threshold 13 V
13	+ 24 V_{DC} IN	24 V_{DC} (20 - 30 V) power supply
14	+ 24 V_{DC} IN	don´t supply with 24 V, when using + 15 V_{DC} supply voltage monitoring threshold 15,6 V
15	U_{DC} analog OUT	U_{DC} when using **option „U”** actual DC-link voltage, 9,0 V refer to U_{DCmax}
16	Temp. analog OUT	max. output current 5 mA
17	GND aux	reference for analog output signals
18	I analog OUT HB 1	current actual value, 8,0 V refer to 100 % I_C overcurrent trip level 10 V ⇔ 125 %; I_C @ 25 °C current value > 0 ⇔ SKiiP is source current value < 0 ⇔ SKiiP is sink
19	I analog OUT HB 2	current actual value, 8,0 V refer to 100 % I_C overcurrent trip level 10 V ⇔ 125 %; I_C @ 25 °C current value > 0 ⇔ SKiiP is source current value < 0 ⇔ SKiiP is sink
20	GND aux	reference for analog output signals

[1)] Open collector output, external pull up resistor necessary
[2)] „high“ (min) 11,2 V, „low“ (max) 5,4 V